AMENDMENTS TO THE SPECIFICATION:

Pages 19-20: please replace paragraph 0037 with the following amended paragraph:

[0037] The sleep mode voltage controller 200 may also be configured to provide a well voltage, such as an n-well voltage V_{nwell}, to the SRAM array during sleep mode. As illustrated, the sleep mode voltage controller 200 provides the high operating voltage V_{DD} to the SRAM array for the n-well voltage during sleep mode. In other embodiments, the sleep mode voltage controller 200 may include additional switches or other controls to selectively provide a well voltage to the SRAM array based on transistor parameters. For example, n-well may be raised relative to the high operating voltage V_{DD} for embodiments having strong corner p-channel transistors. ~~For example, n-well may be connected to a high input/output voltage $V_{DDI/O}$ at about 1.8 volts while the high operating voltage V_{DD} is at about 1.2 volts.~~ Optionally, the first switch 210 and the second switch 220 may be connected to a voltage other than the high operating voltage V_{DD}. For example, the first switch 210 and the second switch 220 may be connected to the high input/output voltage $V_{DDI/O}$. Also, as shown, first diode 250 and second diode 260 may be used to provide a voltage drop from the high operating voltage V_{DD} to the array high supply voltage V_{ADD}. Other circuit elements could be used such as transistors or resistors. Alternatively, a voltage regulator such as an LDO may be used to supply the array high supply voltage V_{ADD}. Similarly, various circuit elements, such as diodes, transistors, and resistors may be used to supply the array low supply voltage V_{ASS}.